UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/072,319 | 02/07/2002 | Yeun-Renn Ting | JCLA8481 | 3211 |

7590 07/22/2004

J.C. Patents, Inc.
4 Venture, Suite 250
Irvine, CA 92618

| EXAMINER | |
|---|---|
| TORRES, JOSEPH D | |
| **ART UNIT** | **PAPER NUMBER** |
| 2133 | 2 |

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/072,319 | TING ET AL. | |
| | Examiner | Art Unit | |
| | Joseph D. Torres | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: '220' in line 3 on page 9. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: '222' in Figure 2. Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

2. Claims 1-18 are objected to because of the following informalities: "A turbo-code decoder for communication system" in line 1 should be changed to: --A turbo-code decoder for **a** communication system--.

As per claim 4, "serial input signal" in line 1 should be replaced with --serial input signal**s**--.

As per claim 5, "coverts" in line 1 should be replaced with --co**n**verts--.

Claim 16 must be rewritten so it is independent of the figures

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites, "with certain sequence, the parallel signal passes through the parallel decoding units for decoding process" in lines 8 and 9, which is incomprehensible.

Claim 2 recites, "when processing the decoding process" in line 2, which is incomprehensible.

Claim 2 recites, "to be the signal that is after the decoding process from the parallel decoding unit" in lines 2 and 3, which is incomprehensible.

As per Claim 3, a0 in the extrinsic parameter $L_{a0,k}$ is undefined.

As per Claim 4, 1s, 1p and 2p in the input signals $r_{1s,k}$, $r_{1p,k}$ and $r_{1p,k}$ are undefined.

Claim 8 recites, "N+M units of the module C, A, B, D, and E". It is not clear whether C, A, B, D, and E is a singe module or five different modules. It is not clear whether there are N+M units of C, N+M units of A, N+M units of B, N+M units of D, N+M units of E or whether there are N+M units of the single module C, A, B, D, and E or whether there are N+M total units of modules from the C modules, A modules, B modules, D modules and E mosules.

4. Claims 5-18 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 5 recites, "M stands for a total number of latch units of the turbo-code decoder". The omitted structural cooperative relationships are: the relationship between "latch units" and "the turbo-code decoder".

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Hladik; Hladik; Stephen Michael et al. (US 6192501 B1, hereafter referred to as Hladik).

35 U.S.C. 102(b) rejection of claim 1.

Hladik teaches a turbo-code decoder for communication system (Figure 6 in Hladik is a turbo-code decoder for a communication system), the decoder comprising: a serial-to-parallel output unit, used to receive a serial input signal and output a parallel signal after converting the serial input signal (col. 4, lines 16-21 in Hladik teach that Composite-Codeword-To-Component-Codeword Converter 22 in Figure 6 of Hladik converts a serial sequence of symbols into parallel signals: Note: the first signal outputted from the Composite-Codeword-To-Component-Codeword Converter 22 is in parallel with the other signals, hence is a parallel signal); and a plurality of parallel decoding units (Decoders 1-N in Hladik are a plurality of parallel decoding units), wherein the parallel decoding units are serially connected to form a plurality of levels (Decoders 1-N in Hladik are serially connected to form a plurality of levels), the first level parallel

decoding unit receives the parallel signal that is output from the serial-to-parallel output unit (Decoder 1 in Figure 6 of Hladik is a first level parallel decoding unit receiving the first parallel signal that is output from the serial-to-parallel output unit Composite-Codeword-To-Component-Codeword Converter 22 in Figure 6), the output from the first level parallel decoding unit is sent to the second level parallel decoding unit (in Figure 6 of Hladik, the output from the first level parallel decoding unit Decoder 1 is sent to the second level parallel decoding unit Decoder 2), with certain sequence, the parallel signal passes through the parallel decoding units for decoding process (Note if the input signals are correct when received, the first parallel signal will pass through parallel decoding units Decoders 1-N in Figure 6 of Hladik, with certain sequence).

35 U.S.C. 102(b) rejection of claim 2.

Hladik teaches each of the parallel decoding unit receives an extrinsic parameter when processing the decoding process, to be the signal that is after the decoding process from the parallel decoding unit, and sends the extrinsic parameter to the next level of the parallel decoding unit ($\lambda_1^e(d_t)$, $\lambda_2^e(d_t)$,..., $\lambda_N^e(d_t)$ in Figure 6 of Hladik are extrinsic parameters).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 3-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hladik; Hladik; Stephen Michael et al. (US 6192501 B1, hereafter referred to as Hladik).

35 U.S.C. 103(a) rejection of claim 3.

Hladik substantially teaches the claimed invention described in claims 1 and 2 (as rejected above).

However Hladik does not explicitly teach the specific use of initializing extrinsic values to zero.

The Examiner asserts that the Extrinsic values $\lambda_1^e(d_t)$, $\lambda_2^e(d_t)$,..., $\lambda_N^e(d_t)$ in Figure 6 of Hladik are required inputs to each of the N Decoders in Figure 6 used to adjust estimates as the decoder iterates through the various stages of the iterative decoding algorithm used for the decoder in Figure 6. Since initially the decoders have no extrinsic information, the extrinsic values must be set so they do not alter the initially received data. It would be obvious to use zero to designate that the initial values not be altered.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hladik by including use of initializing extrinsic values to zero. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of initializing extrinsic values to zero would have provided the opportunity to designate that the initial values not be altered.

35 U.S.C. 103(a) rejection of claim 4.

Hladik substantially teaches the claimed invention described in claims 1-3 (as rejected above).

However Hladik does not explicitly teach the specific embodiment of the turbo encoder of Figure 5.

The Examiner asserts that it would have been an obvious engineering design choice to select a particular embodiment of the turbo encoder of Figure 5 in Hladik based upon requirements for data throughput and desired error rate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hladik by including use of a particular embodiment of the turbo encoder of Figure 5. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a particular embodiment of the turbo encoder of Figure 5 would have provided the opportunity to meet design requirements for data throughput and desired error rate.

35 U.S.C. 103(a) rejection of claim 5.

Hladik substantially teaches the claimed invention described in claims 1-4 (as rejected above). In addition, Hladik teaches the serial-to-parallel output unit converts the received $r_{1s,k}$, $r_{1p,k}$ and $r_{1p,k}$ messages and outputs results to the first level parallel decoding unit in parallel (Composite-Codeword-To-Component-Codeword Converter 22 in Figure 6 of Hladik converts the received $r_{1s,k}$, $r_{1p,k}$ and $r_{1p,k}$ messages and outputs results to the first level parallel decoding unit in parallel), the first level parallel decoding unit also receives an extrinsic parameter $L_{a,k}$ at the same time, the parameter $L_{a,k}$ is obtained via a deinterleaving operation on the previous level extrinsic parameter $\lambda(d_k)$ (in Figure 6 of Hladik, $L_{a,k}$ = deinterleaved $\lambda_N^e(d_t)$ and $\lambda(d_k) = \lambda_N^e(d_t)$), a first level extrinsic parameter $L_{a1,k}$ is generated via the first level parallel decoding unit, and the message $r_{1s,k}$, $r_{1p,k}$ and $r_{1p,k}$ pass through sequentially to be the input of the next level (in Figure 6 of Hladik, $L_{a1,k}$ = interleaved $\lambda_1^e(d_t)$).

However Hladik does not explicitly teach the specific use of initializing extrinsic values to zero.

The Examiner asserts that the Extrinsic values $\lambda_1^e(d_t)$, $\lambda_2^e(d_t)$,..., $\lambda_N^e(d_t)$ in Figure 6 of Hladik are required inputs to each of the N Decoders in Figure 6 used to adjust estimates as the decoder iterates through the various stages of the iterative decoding algorithm used for the decoder in Figure 6. Since initially the decoders have no extrinsic information, the extrinsic values must be set so they do not alter the initially

received data. It would be obvious to use zero to designate that the initial values not be altered.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hladik by including use of initializing extrinsic values to zero. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of initializing extrinsic values to zero would have provided the opportunity to designate that the initial values not be altered.

35 U.S.C. 103(a) rejection of claim 6.

Hladik substantially teaches the claimed invention described in claims 1-5 (as rejected above).

However Hladik does not explicitly teach the specific use of a specific embodiment of the decoder in Figure 6 of Hladik with only two decoders. i.e., N=2. Note if N=2 then, a first decoder 1 in Figure 6 is used to receive the $r_{1s,k}$ and $r_{1p,k}$ messages and the extrinsic parameter $L_{a,k}$ = deinterleaved $\lambda_N^e(d_t)$; a second Decoder N=2, used to receive the $r_{1p,k}$ message and the extrinsic parameter $L_{a1,k}$ = interleaved $\lambda_1^e(d_t)$; an interleaving unit Interleaver 1, located between the first decoder and the second Decoder N=2, used to receive the output of the first Decoder 1; and a deinterleaving unit Deinterleaver N=2, used to connected to the second Decoder N=2, alternately outputs the output of the first decoder and the second decoder.

The Examiner asserts that it would have been an obvious engineering design choice to select a particular embodiment of the turbo encoder of Figure 5 in Hladik based upon requirements for data throughput and desired error rate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hladik by including use of a particular embodiment of the turbo encoder of Figure 5. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a particular embodiment of the turbo encoder of Figure 5 would have provided the opportunity to meet design requirements for data throughput and desired error rate.

35 U.S.C. 103(a) rejection of claim 7.

Hladik substantially teaches the claimed invention described in claims 1-6 (as rejected above).

However Hladik does not explicitly teach the specific use of a systolic array very large scaled integrated (VLSI) circuits structure.

The Examiner asserts that it would have been an obvious engineering design choice to select a particular embodiment of the turbo encoder of Figure 5 in Hladik based upon hardware requirements for data throughput and desired error rate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hladik by including use of a particular embodiment of the turbo encoder of Figure 5. This modification would have been

obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a particular embodiment of the turbo encoder of Figure 5 would have provided the opportunity to meet hardware design requirements for data throughput and desired error rate.

35 U.S.C. 103(a) rejection of claims 8-16.

Hladik substantially teaches the claimed invention described in claims 1-7 (as rejected above).

However Hladik does not explicitly teach the specific use of particular hardware for carrying out the backwards and forwards recursions of the Maximum Likelihood Algorithm.

The Examiner asserts that it would have been an obvious engineering design choice to select a particular embodiment of the turbo encoder of Figure 5 in Hladik based upon hardware requirements for data throughput and desired error rate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hladik by including use of a particular embodiment of the turbo encoder of Figure 5. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a particular embodiment of the turbo encoder of Figure 5 would have provided the opportunity to meet hardware design requirements for data throughput and desired error rate.

35 U.S.C. 103(a) rejection of claims 17 and 18.

See col. 10, lines 15-20 and col. 13, lines 5-11 in Hladik.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133